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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,029	08/26/2003	Kenneth J. Kledzik	2087.303C	2417

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EXAMINER
HA, NATHAN W

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,029	KLEDZIK ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 35-36, 39-40, 42-43, 45-46, 49-53, 54-58, 59-62, and 64-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhakta et al. (US 6,222,739, newly cited, hereinafter, Bhakta) and in view of Lin et al. (US 2003/0122240, newly cited, hereinafter, Lin.)

In regard to claims 35 and 40, 42-43, 45, 51, 55-57, 60-61, 65, and 67, in fig. 8, Bhakta discloses an electronic circuit module comprising:

a carrier 164a, comprising a first integrated circuit mounting location comprising a first mounting pad array, a second integrated circuit mounting location disposed on the opposite side of said first mounting pad array comprising a second mounting pad array, a pin-grid array, and a carrier interface; wherein said first and second mounting pad arrays are conductively coupled with said carrier interface 166b, for example;

first and second integrated circuit packages 168, each comprising a package body comprising an integrated circuit chip and a pin-grid array; wherein said pin grid array of said first and second integrated circuit packages are conductively bonded to said first and second mounting pad arrays; and

a printed circuit board 162 having at least one interconnection pad array coupled to circuitry on said printed circuit and conductively bonded to said carrier interface.

Bhakta teaches using pin-grid-array for electrical connections between the devices. This connection type is as widely used as Ball-grid array connection, but conductive device is solder ball, instead. For instance, Lin, in fig. 2A, discloses an analogous stacking package using BGA connection. This connection provides better contact and facilitates the process of forming it.

Therefore, it would been obvious to one of ordinary skill in the art at the time of the invention was made to substitute the BGA connection as taught by Lin in order to take the advantages as mentioned above.

In regard to claims 36, 47, and 64, wherein individual mounting pads of said first mounting pad array are coupled to individual mounting pads of said second mounting pad array by means of conductive links within said carrier, see Bhakta's fig. 8.

In regard to claim 38, wherein said carrier further comprises a recess at 167 for receiving at least a portion of said first and second integrated circuit packages, see Bhakta's fig. 8.

In regard to claims 39 and 50, wherein said carrier further comprises a semi-rigid laminar substrate having first and second major faces corresponding, respectively, to said first and second integrated circuit mounting locations, see Bhakta's fig. 8.

In regard to claims 46 and 62, Bhakta further discloses a printed circuit board having at least one interconnection pad array coupled to circuitry on said printed circuit and conductively bonded to said carrier interface (figs 8-9 and col. 8, lines 37-42.)

In regard to claim 54, Bhakta discloses at least a second carrier conductively bonded to the board, fig. 8.

In regard to claims 49 and 52-53, 59, Lin, in fig. 3B-3C, further discloses a recess in the substrate in order to reduce the thickness of the whole package.

In regard to claims 58 and 66, Bhakta further discloses the carried has a recess at element 167, fig. 8.

3. Claims 37, 41, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhakta and Lin as applied to claims 35-36, 39-40, 42-43, 45-46, 50-51, 54-58, 60-62, and 64-67 above, and further in view of Shim et al. (US 6,683,377, previously cited, and hereinafter, Shim.)

In regard to claims 3, 15, and 26, Ishii discloses all of the claimed limitations as mentioned above except the carrier comprises a flexible polymeric film. It should be noted that polymeric material is widely used in the art of semiconductor package to protect metal interconnections from exposing to the outside to prevent oxidation or electrical short circuit.

For instance, Shim discloses a package that includes polymeric film 10 as an insulating film to protect core layer 11, for example (see also, col. 2, lines 40-44 and figs. 1B-4.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to include an insulating layer, specifically, polymeric layer, in order to protect metal connection devices.

In regard to claim 41, see the above discussion regarding to claim 49.

4. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhakta and Lin as applied to claim 35 above, and further in view of Ishii (US 5,744,862, previously cited.)

In regard to claim 38, the combination of Bhakta and Lin discloses all of the claimed limitations as mentioned above including a recess in the substrate. This recess, however, does not include a portion of the first integrated circuit as claimed.

Ishii, in fig. 2, for example, discloses an analogous device including a substrate, a first chip and second chip. The substrate further includes a recess wherein the portions of the chips are embedded therein. By having portions of the chips in the recess the thickness of the whole package is significantly reduced.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to include portions of the device in the recess as taught by Ishii in order to take the advantage as mentioned above.

5. Claims 44 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhakta and Lin as applied to claims 35-36, 39-40, 42-43, 45-46, 49-53, 54-58, 59-62, and 64-67 above, and further in view of Herrell et al. (US 6,828,666, newly cited, hereinafter, Herrell.)

In regard to claims 44 and 63, the combination of Bhakta and Lin discloses all of the claimed limitations as mentioned above except the substrate is a ceramic ball-grid array. Herrell discloses an analogous package including multiple chips mounted on a ceramic ball-grid array in order to reduce the difference in thermal coefficient between the substrate and the dies.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to substitute the ceramic substrate as taught by Herrell in order to take the advantage as mentioned above.

Response to Arguments

6. Applicant's arguments with respect to claims 35-67 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nathan Ha
August 10, 2005

HOAI PHAM
PRIMARY EXAMINER